Remarks

Claims 1-5, 7-17 and 19-20 remain in the application. Claims 6 and 18 are hereby canceled without prejudice. Claims 1, 12, 15, 19, and 20 are hereby amended. No new matter is being added.

Double Patenting

Claim 18 was rejected on the basis of nonstatutory double patenting. Claim 18 is hereby canceled without prejudice. As such, applicants respectfully submit that this rejection is now moot.

Claim Rejections -- 35 USC 101

Claim 18-19 were rejected under 35 USC 101. As stated by the Examiner, "The program product needs to be stored on the computer readable medium in order to be acceptable under 35 USC 101."

Claim 18 is hereby canceled without prejudice. Claim 19 is hereby amended to incorporate the limitations of claim 18. Claim 19 is also hereby amended so as to recite, "A computer-readable program product **stored on a computer-readable medium** ...." (Emphasis added.) Hence, applicants respectfully submit that amended claim 19 now overcomes this rejection.

Claim Rejections--35 USC 102

Claims 1-5, 10-14, 16, 17 and 20 were rejected under 35 U.S.C. 102(e) as being anticipated by Quach (USP 6,640,313). The claims rejected in this rejection include independent claims 1, 12, and 20, each of which is hereby amended so as to overcome this rejection.

Independent claim 1 is hereby amended so as to include the limitations from original dependent claim 6 relating to the opportunistic scheduling of redundant operations. Claim 6 is not among the claims rejected under 35 USC 102(e), but rather is rejected under 35 USC 103(a). Hence, the patentability of amended claim 1 and its dependent claims 2-5 and 10-11 are discussed below in relation to the rejection under 35 USC 103(a).

Similarly, independent claim 12 is hereby amended so as to include the limitations from original dependent claim 18 relating to the opportunistic scheduling of redundant operations. Claim 18 is not among the claims rejected under 35 USC 102(e), but rather is rejected under 35 USC 103(a). Hence, the patentability of amended claim 12 and its dependent claims 13-14 and 16-17 are discussed below in relation to the rejection under 35 USC 103(a).

Also similarly, claim 20 is hereby amended so as to include the limitations from original claim 6. the patentability of amended claim 20 is discussed below in relation to the rejection under 35 USC 103(a).

Claim Rejections--35 USC 103

Claims 6-9, 15, 18, and 19 were rejected under 35 U.S.C. 102(e) as being unpatentable over Quach in view of Fruehling (USP 6,625,688). As discussed above, independent claim 1, 12, and 20 are hereby amended and now are appropriately discussed in relation to this rejection. Hence, this rejection is now traversed with respect to all the pending claims.

Claims 1-5 and 7-11

Amended claim 1 now recites as follows.

> 1. A method of providing **opportunistic** functional testing **within a central processing unit (CPU)**, the method comprising:
>
> executing **pre-scheduled redundant and non-redundant operations** on multiple functional units of a same type in the CPU;
>
> automatically comparing outputs from the multiple functional units; and
>
> **checking results of the comparison only for the pre-scheduled redundant operations but not for the pre-scheduled non-redundant operations,**
>
> **wherein the redundant operations are opportunistically scheduled by a compiler to take advantage of an otherwise idle functional unit during a cycle.**

(Emphasis added.)

As seen above, the claimed invention recites providing **opportunistic** functional testing **within a CPU**, where the opportunistic testing is controllable on a **per**

operation basis by **pre-scheduling redundant and non-redundant operations.** Moreover, the claimed invention recites that "**the redundant operations are opportunistically scheduled by a compiler to take advantage of an otherwise idle functional unit during a cycle.**"

In other words, the claimed invention has a **basic operating principle** where **individual operations** are **pre-scheduled by a compiler** to be performed either redundantly or non-redundantly. In other words, the claimed invention operates on an **instruction-based or instruction-dependent principle** in which each operation (instruction) is pre-designated by the compiler to be either redundantly or non-redundantly executed. This principle enables the claimed invention to **opportunistically** take advantage of otherwise idle cycles.

In contrast, the processor of Quach teaches operation on a **mode-based or mode-dependent principle** in that it operates in high-reliability or high-performance modes in response to **mode switch events**. (See first sentence of Abstract of Quach.)

Frueling et al is cited for its disclosure that in a particular state, "the PSA Mode Controller may steal a bus cycle or use idle bus cycles if available." (Fruehling, column 11, lines 32-34.) Applicants respectfully submit that the **bus cycle** pertains to a bus **outside the CPU** and is substantially different from a **processor cycle within the CPU**. Moreover applicants respectfully submit that, like Quach, Fruehling et al teaches operation on a **mode-based or mode-dependent principle**. See, for example, the various modes (states) in FIG. 4 of Fruehling et al.

MPEP 2143.01 states as follows.

> **THE PROPOSED MODIFICATION CANNOT CHANGE THE PRINCIPLE OF OPERATION OF A REFERENCE**
>
> If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959) (Claims were directed to an oil seal comprising a bore engaging portion with outwardly biased resilient spring fingers inserted in a resilient sealing member. The primary reference relied upon in a rejection based on a combination of references disclosed an oil seal wherein the bore engaging portion was reinforced by a cylindrical sheet metal casing. Patentee taught the device required rigidity for operation, whereas the claimed invention required resiliency. The court reversed the rejection holding the "suggested combination of references would require a substantial reconstruction

> and redesign of the elements shown in [the primary reference] as well as a change in the basic principle under which the [primary reference] construction was designed to operate." 270 F.2d at 813, 123 USPQ at 352.).

As seen above, MPEP 2143.01 states, "If the proposed modification or combination of the prior art would **change the principle of operation** of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." (Emphasis added.)

Applicants respectfully submit that the proposed combination of Quach and Frueling et al would **change the principle of operation** of both Quach and Fruehling et al. In particular, the proposed modification would require changing the fault-detection in Quach and Fruehling et al from one operating on a **per mode or mode-dependent basis** to a substantially different mechanism operating on a **per instruction or instruction-dependent basis**. Hence, under MPEP 2143.01, applicants respectfully submit that the teachings of Quach and Fruehling et al are insufficient to render the claimed invention *prima facie* obvious.

For at least the above-discussed reasons, applicants respectfully submit that amended claim 1 is now patentably distinguished over the cited art.

Claims 2-5 and 7-11 depend from claim 1. As such, applicants respectfully submit that claims 2-5 and 7-11 are now patentably distinguished over the cited art for at least the reasons discussed above in relation to claim 1.

Claims 12-17

Amended claim 12 now recites as follows.

> 12. A microprocessor with built-in functional testing capability which is controllable per execution cycle, the microprocessor comprising:
> multiple functional units of a same type;
> registers that receive outputs from the multiple functional units; and
> comparator circuitry that also receives the outputs from the multiple functional units and compares the outputs to provide functional testing **during pre-scheduled redundant operations but not during pre-scheduled non-redundant operations**.

(Emphasis added.)

As seen above, the claimed invention recites a processor with **built-in** functional testing capability, where "comparator circuitry ... compares the outputs to provide functional testing **during pre-scheduled redundant operations but not during pre-scheduled non-redundant operations**." In other words, the functional testing within the processor is controllable on a **per operation** basis by **pre-scheduling redundant and non-redundant operations.**

As discussed in detail above in relation to claim 1, applicants respectfully submit that the proposed combination of Quach and Frueling et al would **change the principle of operation** of both Quach and Fruehling et al. In particular, the proposed modification would require changing the fault-detection in Quach and Fruehling et al from one operating on a **per mode or mode-dependent basis** to a substantially different mechanism operating on a **per instruction or instruction-dependent basis**. Hence, under MPEP 2143.01, applicants respectfully submit that the teachings of Quach and Fruehling et al are insufficient to render the claimed invention *prima facie* obvious.

For at least the above-discussed reasons, applicants respectfully submit that amended claim 12 is now patentably distinguished over the cited art.

Claims 13-17 depend from claim 12. As such, applicants respectfully submit that claims 13-17 are now patentably distinguished over the cited art for at least the reasons discussed above in relation to claim 12.

Claim 19

Amended claim 19 now recites as follows.

> 19. A computer-readable program product stored on a computer-readable medium for execution on a target microprocessor with multiple functional units of a same type, the program product comprising **executable code that includes a redundant operation scheduled on two functional units to take advantage of one of the functional units that would otherwise be idle during a cycle**, wherein the program product is configured to execute on a microprocessor having comparator circuitry to automatically compare outputs of the two functional units.

(Emphasis added.)

As seen above, the claimed invention recites a computer-readable program product stored on a computer-readable medium, where the program product includes "**executable code that includes a redundant operation scheduled on two functional units to take advantage of one of the functional units that would otherwise be idle during a cycle.**" In other words, the executable code controls the fault checking on a **per operation** (per instruction) basis by **pre-scheduling redundant operations.**

As discussed in detail above in relation to claim 1, applicants respectfully submit that the proposed combination of Quach and Frueling et al would **change the principle of operation** of both Quach and Fruehling et al. In particular, the proposed modification would require changing the fault-detection in Quach and Fruehling et al from one operating on a **per mode or mode-dependent basis** to a substantially different mechanism operating on a **per instruction or instruction-dependent basis**. Hence, under MPEP 2143.01, applicants respectfully submit that the teachings of Quach and Fruehling et al are insufficient to render the claimed invention *prima facie* obvious.

For at least the above-discussed reasons, applicants respectfully submit that amended claim 19 is now patentably distinguished over the cited art.

Claim 20

Amended claim 20 now recites as follows.

20. An apparatus for providing **opportunistic** functional testing **within a CPU**, the apparatus comprising:
    means for executing **pre-scheduled redundant and non-redundant operations** on multiple functional units of a same type in the CPU;
    means for automatically comparing outputs from the multiple functional units; and
    means for **checking results of the comparison only for the pre-scheduled redundant operations but not for the pre-scheduled non-redundant operations,**
    wherein **the redundant operations are opportunistically scheduled by a compiler to take advantage of an otherwise idle functional unit during a cycle**.

(Emphasis added.)

As seen above, the claimed invention recites providing **opportunistic** functional testing **within a CPU**, where the opportunistic testing is controllable on a **per operation** basis by **pre-scheduling redundant and non-redundant operations.** Moreover, the claimed invention recites that "**the redundant operations are opportunistically scheduled by a compiler to take advantage of an otherwise idle functional unit during a cycle**."

As discussed in detail above in relation to claim 1, applicants respectfully submit that the proposed combination of Quach and Frueling et al would **change the principle of operation** of both Quach and Fruehling et al. In particular, the proposed modification would require changing the fault-detection in Quach and Fruehling et al from one operating on a **per mode or mode-dependent basis** to a substantially different mechanism operating on a **per instruction or instruction-dependent basis**. Hence, under MPEP 2143.01, applicants respectfully submit that the teachings of Quach and Fruehling et al are insufficient to render the claimed invention *prima facie* obvious.

For at least the above-discussed reasons, applicants respectfully submit that amended claim 20 is now patentably distinguished over the cited art.

Conclusion

For the above-discussed reasons, applicant believes that claims 1-5, 7-17 and 19-20, as they are hereby amended, are now patentably distinguished over the prior art. Favorable action is respectfully requested.

If for any reason an insufficient fee has been paid, the Commissioner is hereby authorized to charge the insufficiency to Deposit Account No. 08-2025.

Respectfully Submitted,

DALE JOHN SHIDLA et al.

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